A 200 MHz 23 mW High-Efficiency Inductive Link Power Supply Circuit with Differential-Driven CMOS Rectifier and Multiple LDOs in 0.18 μm CMOS Process

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ABSTRACT: A 200 MHz CMOS near-field inductive link power supply (ILPS) supplying output power of 18 mW and 5 mW under supply voltage of 1.8 V and 1 V is proposed in this paper. The CMOS power supply consists of differential-driven rectifier and low-dropout regulators (LDOs). Two fully-integrated LDOs with the rectifier produce output voltage 1.8 V and 1 V for supplying analog and digital circuits, respectively. The rectifier has a cross-coupled bridge configuration and is driven by a differential RF input. The simulation output power conversion efficiency (PCE) is 73.7% under 10 mA output current.

1 INSTRUCTIONS

Over the past decades, implantable medical devices (IMDs) have become more and more important in treatment neuropathy. IMDs use electrical pulses to stimulate neural cells and restore neural functions (Kuanfu Chen et al. 2010). Some examples are cochlear implants (P. T. Bhatti et al. 2006), retinal prostheses (A. Rothermel et al. 2009), and closed-loop epilepsy control (W.-M. Chen et al. 2014).

These IMDs are usually supplied through primary batteries and have high power consumption, which consumes more than several mWs. However, batteries store a finite energy and need replacement when depleted, which can be cost-intensive or even not feasible. In order to generate power to be able to supply these IMDS, a stable and reliable power supply is needed essentially (Chung-Yu Wu et al. 2014).

In this paper, we present a power telemetry system (Figure 1) with a near-field inductive link, rectifier, bandgap and LDOs. Section II describes the system architecture and circuit design of the near-field inductive link power supply. The simulation results are shown in Section III, the conclusion is given in Section IV.

2 SYSTEM ARCHTECTURE AND CIRCUIT DESIGN

2.1 The ILPS system

Fig.1 shows the ILPS system which includes near field inductive link coils and regulator. The input energy is transfered to the regulator to produce two stable supply votages 1.8V and 1V by near-field coils (Chung-Yu Wu et al. 2014).

In this paper, we design a 200 MHz CMOS near-field inductive link power supply circuit, which including 7 stages CMOS rectifier, a bandgap reference and two LDOS.

The DC voltages (VDCH and VDCL) are produced from six and single stages rectifier, respectively. Finally we generate two stable supply with power of 18mW and 5mW from LDOs (Kuanfu Chen et al. 2010).
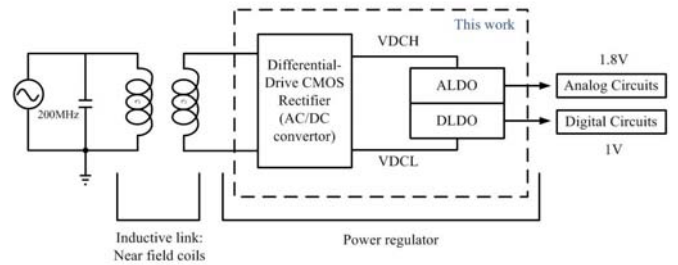

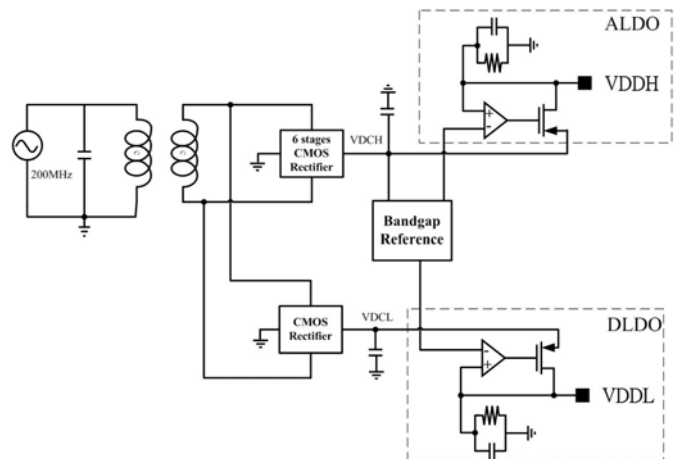Fig.1   The ILPS system.

2.2 The ILPS architecture

Fig.2   Architecture of the 200 MHz CMOS near-field inductive link power supply circuit.

3 SIMULATION RESULTS

3.1 Pre-layout simulation

Fig.3 and Fig.4 show the pre-layout simulation result. Fig.3 shows two output supply voltages. Fig.4 shows two output supply current.
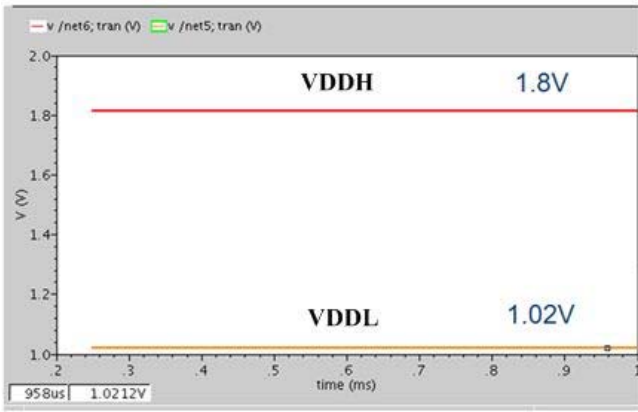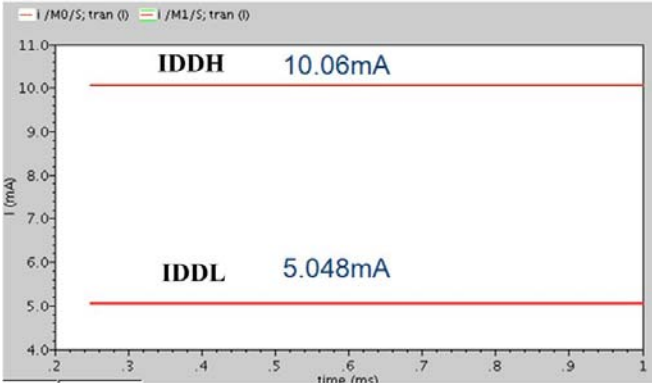
Fig.3   Two output supply voltages(VDDH&VDDL).

Fig.4   Two output supply current.(IDDH&IDDL)

3.2 Post-layout simulation

Fig.5 and Fig.6 show the post-layout simulation result. Fig.5 shows two output supply voltages. Fig.6 shows two output supply current.
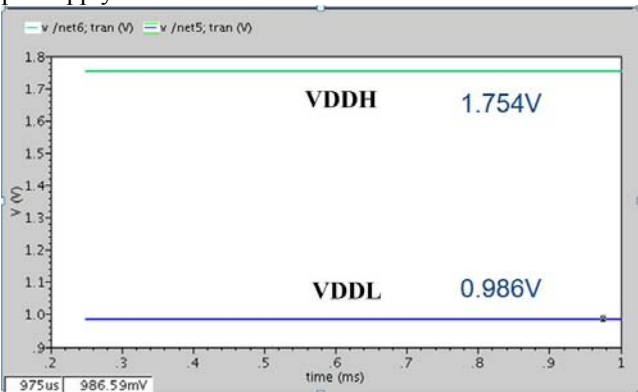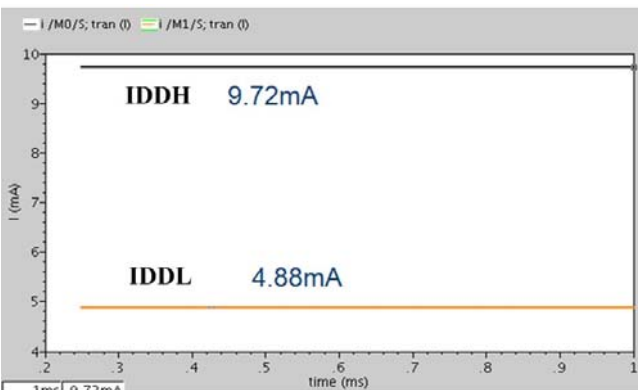

Fig.5   Two output supply voltages(VDDH&VDDL).

Fig.6   Two output supply current.(IDDH&IDDL)

Table.1   The Perfoemance Of The ILPS.

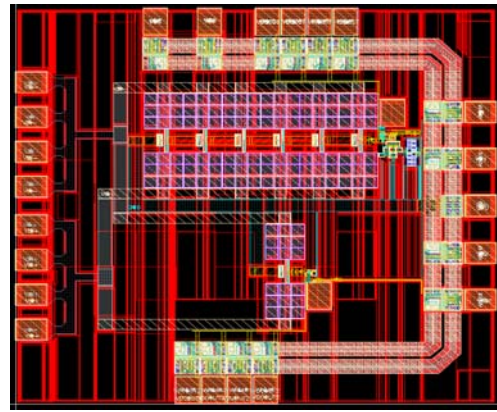| Result	Spec	Pre-sim(tt)	Post-sim(tt)
Output Voltage VDDH(V)	1.8	1.8	1.754
Output Current IDDH(mA)	10	10.06	9.72
Output Voltage VDDL(V)	1	1.02	0.986
Output Current IDDL(mA)	5	5.048	4.88
Total Output Power(mW)	23	23.25	21.86

3.3 Layout

Fig.7   Layout of ILPS circuit.

Layout of the proposed ILPS circuit is shown in Fig. 7.

4 CONCLUSION

In this paper, we design a 200MHz high-efficiency ILPS circuit. It can supply 23mW output power and use multiple LDOs to fit different power needs in different circuits. In simulation, it can generate 1.8V and 1V at ALDO and DLDO. The output current can reach 10mA and 5mA. Overall ILPS can achieve PCE of 73.7% under load of 180Ω.

5 REFERENCES

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