A 2.5-V, 14-bit MASH Sigma-Delta Modulator for ADSL

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ABSTRACT

This work presents a fourth order, multi-stage noise shaped (MASH) sigma-delta modulator (SDM) for wide bandwidth applications. Each stage of the SDM consists of a second order SDM with multi-level quantizer. The first stage is a low distortion second order single loop SDM, while the second stage of the SDM is a low distortion SDM with Chebyshev type II filter technique. The proposed architecture can reduce the signal distortion of circuits to improve the performance. A test SDM chip for ADSL application is designed and implemented by TSMC 0.25um process. The simulation results indicate that the dynamic range (DR) could reach 87dB with power dissipation of 65mW.

1. INTRODUCTION

The high-resolution characteristics of SDM usually attract people. However, the oversampling nature of the SDM restricts the applications of SDMs to audio and measurement fields [1]. As the process technology of VLSI (very large scale integrated circuits) advances, researchers move their attentions on SDM to the wide bandwidth applications such as xDSL, Bluetooth, and GSM [2][3]. The resolution of a SDM is decided by several factors, such as oversampling ratio (OSR), levels of quantizer, and orders of the SDM. Obviously, the OSR of a wide bandwidth application SDM cannot be high. There are several types of architectures for designing a wide bandwidth SDM, such as single loop high order architecture, interpolative architecture, and multi-stage noise shaped (MASH) architecture. For wide bandwidth applications, the single loop SDM and the interpolative SDM need a multi-bit quantizer and thus a multi-bit digital-to-analog converter (DAC) is needed in the feedback loop. However, the linear error of the DAC may degrade the performance of the SDM. In order to reduce the linear error caused by the DAC, correction hardware is needed in the system, such as data weighted averaging (DWA) technique [4]. Theoretically, the non-linear error of a multi-bit DAC in a MASH SDM can be shaped to the out-of band frequency and can have very good performance. Therefore, the MASH architecture is proper to be used in wide bandwidth applications.

In this paper, we propose a SDM for ADSL application. For wide bandwidth applications, the system with higher OSR is not reachable, and therefore a two-stage MASH architecture is used. In order to reduce the mismatch effect, the SDM in each stage of the MASH must be as simple as possible. Besides the mismatch consideration, high resolution and wide bandwidth are two important factors of the SDM design. Therefore, a low distortion technique [5] is applied in both stages. Under these two considerations, the first stage of the MASH architecture is composed of a second order low distortion single loop SDM with multi-bit quantizer. The second stage of the MASH architecture is designed by a second order low distortion interpolative SDM with Chebyshev type II filter technique. Finally, the proposed architecture is implemented by TSMC 0.25um process.

2. SYSTEM DESIGN

This work proposes a two-stage fourth order MASH SDM, and each stage is composed of a second order SDM. A low distortion second order SDM and a low distortion second order interpolative SDM are used in our design. The details of the architectures are discussed in the following subsections.

2.1 Single loop low distortion SDM

The block diagram of a single loop SDM is shown in Figure 1. In this architecture, the harmonic distortion of the input signal, *X*, caused by the swing limitation of the circuit may propagate to the output of the SDM. Silva et al. [5] proposed a new SDM architecture, called low distortion SDM, which can solve the harmonic distortion problems. The block diagram of a low distortion SDM is shown in Figure 2. The signal transfer function (STF) of this SDM is equal to unity, and the input signal, *X*, is thus canceled in the first summer and will not appear in block L. This feature makes the system to be no signal delay and thus can operate with low distortion.

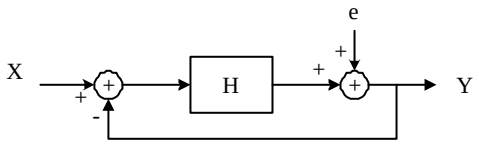

Figure 1. Conventional single-loop SDM architecture

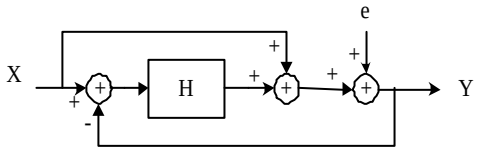

Figure 2. Low-distortion SDM architecture

For low OSR SDM, the non-linear gain is a critical factor to reduce the circuit performance. The non-linear gain of an opamp can be represented as equation (1) [7]. It is assumed that the non-linear effect is dominated by the output swing

of the operational amplifier. In the low distortion SDM architecture, the output swing of each integrator in block H is small and only the quantization noise may distribute. This can prove that the low distortion architecture has less distortion due to the non-linear gain of the opamp:

$$A = A_0\left(1 + a_1 v_o + a_2 v_o^2\right), \qquad (1)$$

where v_o is the output of the operational amplifier. For a reasonable output swing of each integrator, the low distortion SDM must use a multi-bit quantizer. From the MATLAB simulation, the bit number of the quantizer has to be 2 or more.

2.2 The proposed MASH SDM architecture

According to the previous work [10], we used an interpolative SDM in the second stage to gain the system bandwidth for wide bandwidth applications. In this work, the first stage, shown in Figure 3, uses a single loop low distortion second order SDM. The second stage uses an interpolative SDM.

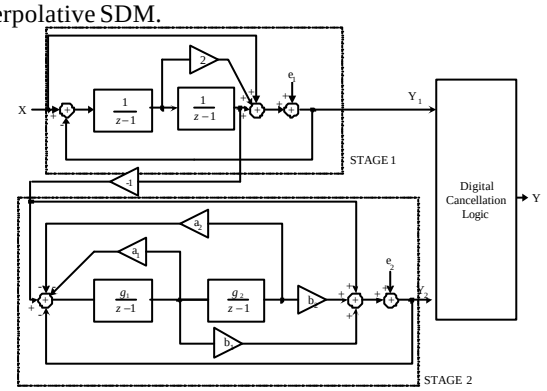

Figure 3. The proposed MASH SDM

Since we can decide the poles and zeros of an interpolative SDM, the bandwidth of the SDM can be found by determining the locations of the zeroes. The interpolative SDM is similar to a filter, and therefore there are several types of filters that can be used. The proposed work uses the Chebyshev type II filter as the base of the interpolative SDM. Here, the coefficients of the Chebyshev type II filter are chosen such that the filter has flatten pass band and clear stop band [6]. The transfer function of the loop filter in the second stage can be derived as follows:

$$\frac{\text{Out}}{\text{In}} = \frac{b_1 g_1 z + (b_2 g_1 g_2 - b_1 g_1)}{z^2 + (a_1 g_1 - 2)z + (a_2 g_1 g_2 - a_1 g_1 + 1)}. \qquad (2)$$

In order to reduce the harmonic distortion of the system, the second order Chebyshev type II SDM is revised to become a low distortion SDM.

2.3 Consideration of the multi-bit quantization

Because the multi-bit quantization is needed to keep the reasonable swing of the loop filter in the low distortion architecture, the non-linearity of the feedback DAC has to be discussed. The non-linearity of the feedback DAC is caused by the process variation of resistors or capacitors. Typically, the variation rates of resistors and capacitors are about 1% and 0.1%, respectively; furthermore, they severely depend on the process of technology. In [4], Baird et al. proposed a new dynamic-element-matching (DEM) algorithm, called DWA, to use all the DAC elements at the maximum possible rate while ensuring that each element is used in the same number of times. With this algorithm, the first-order noise shaping shapes the distortion spectrum of the DAC non-linearity to out-of band of the bandwidth. For the MASH SDM, the DAC non-linearity of the second stage is reduced by the followed digital cancellation logic. Therefore, the first DAC is the most critical block of the non-linearity. The results of the non-ideality simulated by MATLAB are listed in Table 1. In Table 1, it shows that the DWA technique used in the first stage is useful. However, the DWA used in the second stage does not improve the circuit.

3. Circuit Implementation

We use a fully differential approach to implement the proposed SDM. A fully differential folded-cascode opamp with techniques of PMOS-input differential pair and dynamic CMFB is chosen for the low noise and stable output common mode level. Each of the quantizer is a nine-level flash ADC for adapted output swing in each integrator. Figures 5, 6, and 7 show the schematics of the integrator with DAC, quantizer, and analog summer, respectively.

Table 1. The SNDR of the proposed SDM simulated by Matlab with sampling capacitor = 4pF in the first integrator, finite DC gain = 1000, and settling error = 0.1%. These are calculated by 4096-point FFT with Blackman window.

SNDR (dB)	Without DWA			With DWA (in 1st stage)			With DWA (in 2nd stage)		
	Min	Max	Avg	Min	Max	Avg	Min	Max	Avg
Without Mismatch (100 samples)	86.19	89.98	88.02	86.19	89.98	88.02	86.19	89.98	88.02
With Mismatch (0.1%, 100 samples)	65.65	83.56	**75.53**	86.54	89.65	**88.11**	68.20	85.75	**76.00**

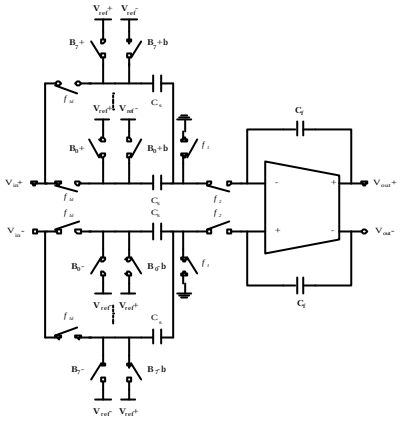

Figure 5. Integrator with DAC

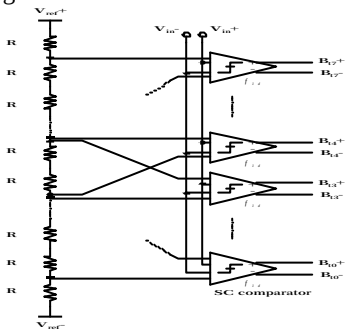

Figure 6. Quantizer

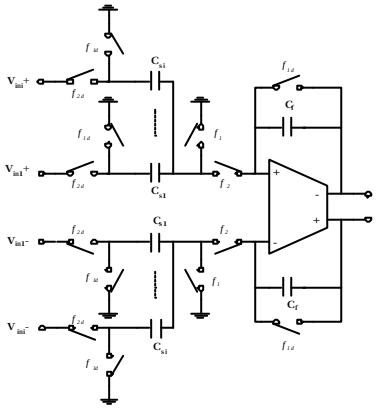

Figure 7. Analog summer

4. SIMULATION RESULTS AND COMPARISONS

Based on the proposed SDM architecture, a SDM for ADSL application is designed and simulated by TSMC 0.25um process. According to the specifications of ADSL, the coefficients of the Chebyshev type II filter, g_1=g_2=1, a_1=a_2=0.068, b_1=2.844, and b_2=2.167, are found by MATLAB. The proposed SDM is simulated by MATLAB and HSPICE. Figure 8 shows the output swing histogram of each opamp with –6dB amplitude (v_{ref}=0.5v). The swing of each output of integrator is quite small to keep good linearity. The power spectrum, shown in Figure 9, with a sinusoidal wave (v_m=0.4v and f_{in}=397kHz) is simulated by HSPICE and calculated by MATLAB with 1024-point FFT and Blackman window. Figure 10 indicates that the dynamic range of the proposed SDM is about 87dB. Table 2 lists three performances of the proposed SDM with Gaussian distribution resistors and capacitors. The conditions of the mean and variance are from the reference book of TSMC 0.25 um process. The specification comparisons of the SDM and other wide bandwidth SDM are shown in Table 3. The IC microphotograph is shows in Figure 11. The measured modulator output PSD is shown in Figure 12. It shows the cumulative noise and the distortion noise.

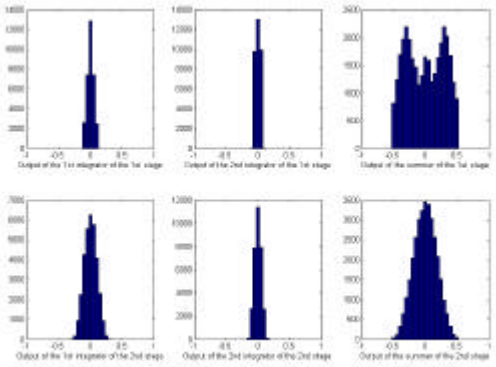

Figure 8. Output swing histogram of each opamp

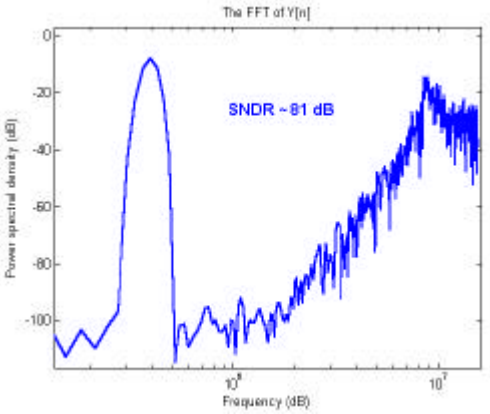

Figure 9. Power spectrum of the proposed SDM

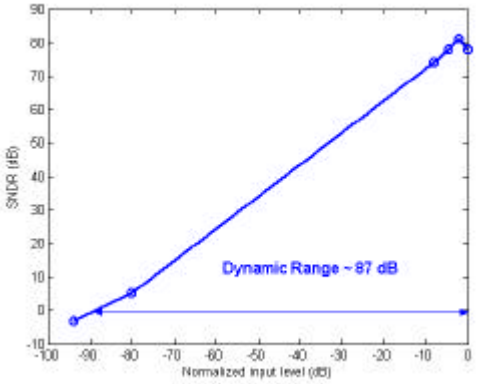

Figure 10. Dynamic range of the proposed SDM

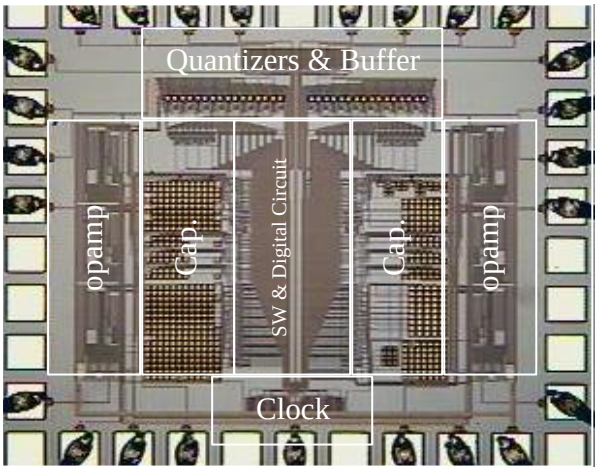

Figure 11. IC microphotograph

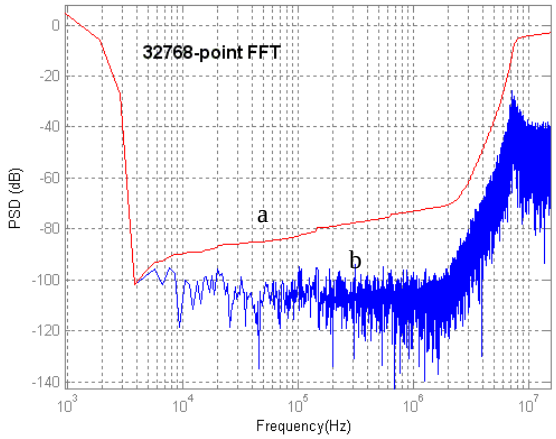

Figure 12. The measured modulator output PSD without signal, both cumulative noise power (line-a) and distortion noise (line-b) are shown.

Table 2 Monte Carlo analyses with 0.1% mismatch

	1	2	3	Average
SNDR (dB)	70.7290	75.0624	78.2506	74.68
P_{diss} (mW)	65.083	65.059	65.082	65.075

Table 3. Wide bandwidth SDM specification comparisons

Ref.	[8](Measured)	[9](Measured)	***Post-layout simulation***
DR	90dB	84dB	***87dB***
PSNDR	82dB	80dB	***81dB***
BW	1.1MHz	1.25MHz	***1.25MHz***
Fs	52.8MHz	30MHz	***30MHz***
OSR	24	12	***12***
P_{diss}	200mW	100mW	***65mW***
Area	$5mm^2$	$2.6mm^2$	***$1.28mm^2$***
V_{supply}	3.3v	2.5v	***2.5v***
Technology	0.5um	0.25um	***0.25um***

5. CONCLUSION

In this paper, a two-stage fourth order MASH SDM for wide bandwidth application is proposed. In order to achieve the high-resolution requirement, the low distortion technique is applied in both stages. For wide bandwidth considerations, multi-bit quantization and Chebyshev type II filter techniques are applied in this SDM. Based on the proposed architecture, a SDM for ADSL applications is designed and simulated. The DR of the designed SDM is 87dB with OSR=12, and the power consumption is 65mW.

6. REFERENCES

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